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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/755,734	01/12/2004	Roger D. Isaac	5500-91000	1103

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/755,734	ISAAC ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received October 12, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Information Disclosure Statement(s) is being considered by the examiner.

Claim Objections

2. Claim 3, line 1 is objected to because it is unclear what "scheduler" refers to. Applicant is advised to change this language to "said scheduler".

Claim 20, line 1 is objected to because it is unclear what "scheduler" refers to. Applicant is advised to change this language to "said scheduler".

Claims 18-25 are objected to because of the following informalities:

The applicant has provided two claims that are numbered identically (claim 18), the first of which is an independent claim and the second of which appears to be dependant thereupon. The second, dependant claim as well as the remaining claims that depend upon either of these two claims should be renumbered, as should respective dependencies of all of these claims. Appropriate correction is required.

For the purposes of this action, the second, dependant claim 18 will be assumed to be claim 19, and its dependency assumed to be upon the first, independent claim 18, and the remaining claims and their respective dependencies shall follow in a similar

manner. Specifically, claims 19-25 are now considered as claims 20-26, and their dependencies are changed for consideration accordingly.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 4-8, 10, 15-18 and 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Mudgett et al (US Patent No. 6,775,749).

For claim 1, Mudgett discloses a cache memory subsystem (caches coupled to receive data from a shared memory, col. 2, lines 57-58) comprising:

a cache storage configured to store a plurality of cache lines of data (col. 2, lines 57-58);

a scheduler configured to schedule reads and writes of information associated with a cache storage using a fixed latency pipeline (memory request queue and response queue may be controlled by a queue controller, col. 9, lines 28-30; various stages of an instruction processing pipelines complete their tasks, col. 17, lines 41-42);

wherein in response to scheduling a read request a scheduler is further configured to cause an associated write to occur a fixed number of cycles after

scheduling a read request (a read transaction may be initiated, and a write transaction may be requested after, in which case the system may send a request to the requesting processor and an associated write data may be transferred a programmable number of clocks later, col. 8, lines 59-67 and col. 9, lines 1-13).

For claim 4, Mudgett discloses an associated write corresponds to a cache line of fill data from a system memory (a cache fill in a shared memory system may include a cache fill request, sending a probe to a request, and a speculative response, col. 4, lines 11-17; a probe may also help a processor requesting a cache line so that it can perform a write, col. 9, lines 48-58).

For claim 5, Mudgett discloses a scheduler is further configured to perform an associated write to a storage location within a cache storage having an address corresponding to a read request (a write transaction may be requested and the associated write data transferred over a memory bus to a data buffer or directly to memory, col. 9, lines 6-13).

For claim 6, Mudgett discloses a read transaction may be initiated by a processor sending a read command to a memory via a chipset, and when the chipset is ready to return data, a response may be sent to alert the processor that data is coming, and the data may be provided directly from memory to processor a programmable number of clocks after a response is generated (col. 8, lines 59-67 and col. 9, lines 1-4).

For claim 7, Mudgett discloses a scheduler is further configured to provide an indication a predetermined amount of time before a read response (a cache coherency mechanism may be configured to provide a speculative response to a request to

provide data from a memory to the cache, col. 3, lines 35-50; the amount of delay to insert between sending a probe and launching a speculative response may be determined, and a delay setting may be chosen, col. 8, lines 33-40).

For claim 8, Mudgett discloses a predetermined amount of time is programmable (a delay setting may also be programmable, col. 8, lines 33-46).

Claim 10 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 15 is rejected using the same rationale as for the rejection of claim 6 above.

Claim 16 is rejected using the same rationale as for the rejection of claim 7 above.

Claim 17 is rejected using the same rationale as for the rejection of claim 8 above.

For claim 18, Mudgett discloses a microprocessor (cache controllers may be integrated with a respective processor, col. 3, lines 24-29) comprising:

an execution unit configured to execute instructions and operate on data (a cache coherency mechanism may be configured to receive requests, send probes to cache controllers, and provide speculative responses, col. 3, lines 35-48); and

a lower-level cache subsystem coupled to a higher-level cache subsystem (a processor with a number of different levels of caches, for example, a "level one" (L1) cache and a "level two" (L2) cache, and that these caches may be integrated on the same substrate as the microprocessor, col. 1, lines 16-19).

Claim 23 is rejected using the same rationales as for the rejections of claims 6 and 18 above.

Claim 24 is rejected using the same rationales as for the rejections of claims 7 and 23 above.

Claim 25 is rejected using the same rationales as for the rejections of claims 8 and 24 above.

Claim 26 is rejected using the same rationale as for the rejection of claim 18 above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mudgett et al (US Patent No. 6,775,749), in view of Cypher (US Patent No. 6,629,205).

For claim 9, Mudgett discloses the invention as per rejection of claim 1 above. Mudgett does not, however, expressly disclose a tag storage configured to store a plurality of tags each corresponding to a respective cache line of a plurality of cache lines.

Cypher, however, discloses each line in the cache has associated with it an address tag that is used to uniquely identify the address of the line, and the address tags are included within a tag array memory device (col. 1, lines 28-31).

Mudgett and Cypher are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include tags each corresponding to respective cache lines and a storage for such, because this would allow each line in the cache to have associated with it an address tag to uniquely identify the address of each line, and a means of storing such tags (col. 1, lines 28-30), as taught by Cypher.

7. Claims 2-3, 11-14 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mudgett et al (US Patent No. 6,775,749), in view of Van Doren et al (US Patent No. 6,202,126).

For claim 2, Mudgett discloses the invention as per rejection of claim 1 above. Mudgett does not, however, expressly disclose a cache line of victim data which has been evicted from a higher-level cache.

Van Doren, however, discloses evicted data referred to as "victim" data should be written into main memory, so that storage space is released in a cache (col. 10, lines 15-30).

Mudgett and Van Doren are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been

obvious to a person of ordinary skill in the art at the time of the invention to include victim data being evicted from a cache because this would allow for the CPU to displace stored data to make room for more requested data (col. 10, lines 11-15), as taught by Van Doren.

For claim 3, Mudgett and Van Doren disclose the invention as per claim 2 above. Van Doren further discloses a scheduler is further configured to perform said associated write to a storage location within a cache storage having an address corresponding to a cache line of victim data (a cache control includes a victim address file, which stores the addresses of data elements stored in each victim data buffer, col. 8, lines 8-17).

Claim 11 is rejected using the same rationale as for the rejection of claim 2 above.

Claim 12 is rejected using the same rationale as for the rejection of claim 3 above.

Claim 13 is rejected using the same rationale as for the rejection of claim 4 above.

Claim 14 is rejected using the same rationale as for the rejection of claim 5 above.

Claim 19 is rejected using the same rationales as for the rejections of claims 2 and 18 above.

Claim 20 is rejected using the same rationales as for the rejections of claims 3 and 19 above.

Claim 21 is rejected using the same rationales as for the rejections of claims 4 and 18 above.

Claim 22 is rejected using the same rationales as for the rejections of claims 5 and 21 above.

Citation of Pertinent Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lyon (US PGPub No. 20030154345), discloses a unified tag subsystem for a multilevel cache memory system, which includes lower and upper level hit logics.

Arimilli et al (US Patent No. 6,418,516), discloses a method of operating a multi-level memory hierarchy of a computer system, including speculative requests and upper and lower level cache management.

Contact Information

9. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

3-10-06

PIERRE VITAL
PRIMARY EXAMINER